Adaptive cache insertion policies

Patrycja Balik

December 3, 2019
During this seminar so far, we talked about cache organization, or how things are structured within the cache, e.g. the number of sets and lines, block size.

Today, we’ll focus on cache policies which describe how a cache should work, e.g. write-back vs write-through; write-allocate vs no-write-allocate; inclusive, exclusive or neither; line replacement, etc.
A quick look at cache organization again

<table>
<thead>
<tr>
<th>Set 0:</th>
<th>Set 1:</th>
<th>Set S-1:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valid</td>
<td>Tag</td>
<td>0 1</td>
</tr>
<tr>
<td>Valid</td>
<td>Tag</td>
<td>0 1</td>
</tr>
</tbody>
</table>

\[S = 2^e \text{ sets}\]

Cache size: \[C = B \times E \times S \text{ data bytes}\]

\[1 \text{ valid bit per line} \quad \text{t tag bits per line} \quad B = 2^b \text{ bytes per cache block}\]

\[E \text{ lines per set}\]

Address: \[t \text{ bits} \quad s \text{ bits} \quad b \text{ bits}\]

\[m-1 \quad \text{Tag} \quad \text{Set index} \quad \text{Block offset}\]
The need for eviction is obvious: the cache is smaller than the storage below it in the memory hierarchy.

Requested data isn’t in cache and the set is full $\rightarrow$ a line needs to be evicted to make room for the new data.
Cache replacement policy

Which line to pick for eviction is a matter of replacement policy. The strategy used can have a profound impact on performance.

The choice is a matter of balancing out metadata size overhead, implementation complexity and resulting performance.
Cache replacement policy

- (Pseudo-)Random
- Round-Robin
- FIFO (first in first out)
- LRU (least recently used)
- Pseudo-LRU
- ...
Random

The victim line is chosen randomly, for a good enough definition of random.
The victim line is chosen randomly, for a good enough definition of random.

```c
int getRandomNumber()
{
    return 4;  // chosen by fair dice roll.
    // guaranteed to be random.
}
```

Figure: Not a good PRNG
A counter global for the entire cache determines which line is going to be evicted. Metadata overhead is minimal, and complexity is low, though behavior might not be optimal for code with good locality.
Lines are evicted on a per-set basis. Additional metadata in every set, simple implementation.
Pick the least recently used line for eviction. Good idea, but metadata overhead is high. (Store line age in each line? Encode permutation in set?).
Pseudo-LRU

LRU is good, but complicated—we can try to approximate it. Some approaches, for an n-way cache:

- A variation of random: just store the half in which the LRU is (1 bit)
- Bit-PLRU (n bits)
- Tree-PLRU (n-1 bits)
- ...

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For each line, an additional bit is stored. At the beginning, they’re all 0. When a line is accessed, its bit gets set to 1. If this were to give us 1s in every line in the set, the other lines are reset to 0.

A victim is choosen among the lines with this bit set to 0.
For each set store a sequence representation of a path in a binary search tree, where 0 means "go left" and 1 means "go right".

Leaves represent cache lines, and the path identifies the victim.

On access to line n, flip bits on the path to n in the sequence.
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Tree-PLRU

The diagram represents a Tree-PLRU structure with nodes labeled 0, 1, a, and b. The structure is a tree with nodes branching out, indicating the caching strategy for different elements or data.
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Tree-PLRU

```
0 1
a bc
```
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Tree-PLRU
Fun as that was, it’s easy to show that this is not "true" LRU.
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Tree-PLRU
Thrashing

When the working set is too large for the cache, the cache will thrash by constantly attempting to catch up with the working set, only to need the previously evicted data brought in again.
Adaptive insertion policies

Adaptive Insertion Policies for High Performance Caching

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Hudson, MA
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Simulated cache configuration

<table>
<thead>
<tr>
<th>Cache</th>
<th>Size</th>
<th>Block size</th>
<th>Ways</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1-I</td>
<td>16kB</td>
<td>64B</td>
<td>2-way</td>
</tr>
<tr>
<td>L1-D</td>
<td>16kB</td>
<td>64B</td>
<td>2-way</td>
</tr>
<tr>
<td>L2 (LLC)</td>
<td>1MB</td>
<td>64B</td>
<td>16-way</td>
</tr>
</tbody>
</table>

- Non-inclusive, non-exclusive.
- Unless said otherwise, traditional LRU replacement is assumed.
- We’ll analyze access patterns to the L2 cache.
Dissecting cache replacement

A replacement policy contains two distinct parts: an eviction (victim selection) policy and an insertion policy.

The eviction policy is responsible for choosing a victim when space needs to be freed up in a set, e.g. picking LRU in the LRU replacement policy.

The insertion policy is responsible for where a new line is ordered among the rest at the point it’s added, e.g. at the most recently used (MRU) position in traditional LRU replacement.
In principle, MRU insertion seems like a good idea; it gives blocks a chance to be used before they get evicted from the cache.

However, MRU insertion contributes to the effect of thrashing: a block can be inserted, pass through all the positions and get evicted, without ever being accessed.

For a working set exceeding the cache size, most blocks will just pass through the cache in this manner, leading to a cache miss ratio of 100%.
MRU insertion policy: Zero Reuse Lines

Figure: Zero Reuse Lines for 1MB 16-way L2 cache
## MRU insertion policy: Cache misses I

<table>
<thead>
<tr>
<th>Name</th>
<th>FFWD</th>
<th>MPKI</th>
<th>Compulsory Misses</th>
</tr>
</thead>
<tbody>
<tr>
<td>art</td>
<td>18.25B</td>
<td>38.7</td>
<td>0.5%</td>
</tr>
<tr>
<td>mcf</td>
<td>14.75B</td>
<td>136</td>
<td>1.8%</td>
</tr>
<tr>
<td>twolf</td>
<td>30.75B</td>
<td>3.48</td>
<td>2.9%</td>
</tr>
<tr>
<td>vpr</td>
<td>60B</td>
<td>2.16</td>
<td>4.3%</td>
</tr>
<tr>
<td>facerec</td>
<td>111.75B</td>
<td>3.66</td>
<td>4.8%</td>
</tr>
<tr>
<td>ammp</td>
<td>4.75B</td>
<td>2.83</td>
<td>5.0%</td>
</tr>
<tr>
<td>galgel</td>
<td>14B</td>
<td>5.34</td>
<td>5.9%</td>
</tr>
<tr>
<td>equake</td>
<td>26.25B</td>
<td>18.4</td>
<td>14.2%</td>
</tr>
</tbody>
</table>

**Figure:** FFWD - fast-forward interval, MPKI - misses/kiloinstruction, B - billion
# MRU insertion policy: Cache misses II

<table>
<thead>
<tr>
<th>Name</th>
<th>FFWD</th>
<th>MPKI</th>
<th>Compulsory Misses</th>
</tr>
</thead>
<tbody>
<tr>
<td>bzip2</td>
<td>2.25B</td>
<td>2.4</td>
<td>14.8%</td>
</tr>
<tr>
<td>parser</td>
<td>66.25B</td>
<td>1.57</td>
<td>20.0%</td>
</tr>
<tr>
<td>sixtrack</td>
<td>8.5B</td>
<td>0.42</td>
<td>20.7%</td>
</tr>
<tr>
<td>apsi</td>
<td>3.25B</td>
<td>0.32</td>
<td>21.4%</td>
</tr>
<tr>
<td>lucas</td>
<td>2.5B</td>
<td>16.2</td>
<td>41.6%</td>
</tr>
<tr>
<td>mgrid</td>
<td>3.5B</td>
<td>7.73</td>
<td>46.6%</td>
</tr>
<tr>
<td>swim</td>
<td>3.5B</td>
<td>23.0</td>
<td>50.4%</td>
</tr>
<tr>
<td>health</td>
<td>0B</td>
<td>61.7</td>
<td>0.73%</td>
</tr>
</tbody>
</table>

**Figure:** FFWD - fast-forward interval, MPKI - misses/kiloinstruction, B - billion
LRU insertion policy (LIP)

Idea: modify the insertion policy so that some blocks may be retained and reused in the 100% MR scenario from earlier.

Attempt #1: insert in the LRU position instead of the MRU.

Sounds too simple? Well, it actually helps! Somewhat.
LRU insertion policy (LIP)

Attempt #1: insert in the LRU position instead of the MRU.

The implementation is almost identical to LRU, or any PLRU variant—the only change is skipping the recency update on insertion, no additional overhead required.
LRU insertion policy (LIP)

Problem: LIP doesn’t respond well to changes in working set; old blocks will linger in cache despite not being needed anymore, because there’s no block "aging".

Attempt #2: modify LIP so that occasionally, a block is inserted in MRU position.
Bimodal insertion policy (BIP)

Attempt #2: modify LIP so that occasionally, a block is inserted in MRU position.

Come bimodal insertion policy (BIP), which has a probability $\epsilon$ of using MRU insertion, or LIP otherwise, for a small value of $\epsilon$. For the purpose of data displayed later in this presentation $\epsilon = 1/32 = 0.03125$.

This combines the best of both worlds; adapting to working set changes and thrashing protection.
Case studies: thrashing workloads

First, we’ll analyze benchmarks where LIP and BIP provide a significant improvement over traditional LRU.

These benchmarks are:

- mcf (single-depot vehicle scheduling in public mass transportation)
- art (neural network recognizing objects in a thermal image)
- health (health care system simulation—working set increases with time)
Case study: mcf

```c
while (arcin) {
    tail = arcin->tail;
    if (tail->time + arcin->org_cost > latest) {
        arcin = (arc_t *)tail->mark;
        continue;
    }
    ...
    arcin = (arc_t *)tail->mark;
}
```

Listing 1: **Bold** instructions cause 84% of all cache misses in mcf.

mcf’s behavior can be approximated by a linked list traversal of about 3.5MB of data.
Case study: mcf

Figure: MPKI with the LRU replacement policy for mcf for various L2 sizes.
Case study: mcf

<table>
<thead>
<tr>
<th>Policy</th>
<th>MPKI</th>
<th>Reduction over LRU</th>
</tr>
</thead>
<tbody>
<tr>
<td>LRU</td>
<td>136</td>
<td>-</td>
</tr>
<tr>
<td>LIP/BIP</td>
<td>115</td>
<td>17%</td>
</tr>
<tr>
<td>Optimal</td>
<td>101</td>
<td>26%</td>
</tr>
</tbody>
</table>

**Figure**: Results for the 1MB L2 cache. LIP/BIP retain around 1MB of the working set.
Case study: art

```plaintext
numf1s = lwidth*lheight; // = 100*100 for ref input set
numf2s = numObjects + 1; // = 10 + 1 for ref input set
...
for (tj = spot; tj < numf2s; ++tj) {
    Y[tj].y = 0;
    if (!Y[tj].reset) {
        for (ti = 0; ti < numf1s; ++ti) {
            Y[tj].y += f1_layer[ti].P * bus[ti][tj];
        }
    }
}
Listing 2: **Bold** instructions cause 39% and 41% of L2 misses, respectively.
```
Case study: art

**Figure:** MPKI with the LRU replacement policy for art for various L2 sizes.
Case study: art

<table>
<thead>
<tr>
<th>Policy</th>
<th>MPKI</th>
<th>Reduction over LRU</th>
</tr>
</thead>
<tbody>
<tr>
<td>LRU</td>
<td>38.7</td>
<td>-</td>
</tr>
<tr>
<td>LIP</td>
<td>23.6</td>
<td>39%</td>
</tr>
<tr>
<td>BIP</td>
<td>18.0</td>
<td>54%</td>
</tr>
<tr>
<td>Optimal</td>
<td>12.8</td>
<td>67%</td>
</tr>
</tbody>
</table>

**Figure:** Results for the 1MB L2 cache. Note the differences for LIP and BIP.
Case study: health

```c
while (list != NULL) {
    ...
    p = list->patient;
    ...
    list = list->forward;
}
```

Listing 3: **Bold** is responsible for 71% of all L2 misses.

The health benchmark performs a linked list traversal with frequent insertions and deletions. The size of the working set increases with time.
Case study: health

To display these changes, the program can be split into a few phases, around 50M instructions each.

Figure: MPKI with the LRU replacement policy for health with various L2 sizes.
Case study: health

<table>
<thead>
<tr>
<th>Policy</th>
<th>MPKI</th>
<th>Reduction over LRU</th>
</tr>
</thead>
<tbody>
<tr>
<td>LRU</td>
<td>61.7</td>
<td>-</td>
</tr>
<tr>
<td>LIP</td>
<td>38.0</td>
<td>38.5%</td>
</tr>
<tr>
<td>BIP</td>
<td>39.5</td>
<td>36.0%</td>
</tr>
<tr>
<td>Optimal</td>
<td>34.0</td>
<td>45.0%</td>
</tr>
</tbody>
</table>

**Figure**: Results for the 1MB L2 cache.
LIP and BIP vs LRU

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Case study: swim

swim - performs weather prediction. Heavy on matrix multiplication (but it’s in Fortran, so I haven’t checked).
Case study: swim

Figure: MPKI for swim with LRU. (log scale size axis)
Case study: swim

<table>
<thead>
<tr>
<th>Policy</th>
<th>MPKI</th>
<th>Reduction over LRU</th>
</tr>
</thead>
<tbody>
<tr>
<td>LRU</td>
<td>23.0</td>
<td>-</td>
</tr>
<tr>
<td>LIP</td>
<td>46.5</td>
<td>-102.0%</td>
</tr>
<tr>
<td>BIP</td>
<td>44.3</td>
<td>-92.5%</td>
</tr>
<tr>
<td>Optimal</td>
<td>22.8</td>
<td>0.9%</td>
</tr>
</tbody>
</table>

*Figure:* Results for the 1MB L2 cache.
Dynamic insertion policy (DIP)

Problem: BIP performs very poorly for workloads which benefit from MRU insertion.

Attempt #3: a hybrid solution which picks between traditional LRU, with MRU insertion, and BIP, depending on which causes fewer misses.

Problem: how do we determine which is better at runtime?

Attempt #3.1: For every set analyze misses caused by either policy, modifying a counter global for all sets, and pick a single best policy to use for all sets.
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**DIP-Global**

**Figure:** DIP-Global with 8 sets

MTD - Main Tag Directory

ATD - Auxiliary Tag Directory

PSEL - Policy Selector

(saturating counter)
Problem: the overhead of two extra tag directories isn’t acceptable.

Attempt #3.2: Sample just a select few sets to reduce the size of ATDs.
Problem: while the storage overhead is smaller, major changes still need to be made to the cache organization. Can we avoid this?

Attempt #3.3: for each of the two policies select a few sets that will use them, and use the best policy for the remaining sets. We’ll call this Set Dueling.
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Set Dueling
Set Dueling

Selecting the dedicated sets for DIP-SD...

- ...statically at design time?
- ...dynamically at runtime?
Authors propose the following scheme:

- \( N \) - total number of sets.
- \( K \) - number of sets dedicated to each policy.
- The cache is logically divided into \( K \) constituencies, each containing \( N/K \) sets.
- From each constituency, dedicate one set to each of the competing policies.
- Generally assume that \( K \) is a power of 2 for the purpose of the study.
Complement-select policy

- Out of \( \log_2(N) \) set index bits, let the most significant \( \log_2(K) \) bits identify the constituency and the remaining \( \log_2(N/K) \) the offset from the first set in the constituency.
- (Yes, at this point "constituency" stops looking like a real word.)
Complement-select policy

\[ \log_2(K) \]
\[ \log_2(N/K) \]

Constituency identifier
Offset from first in constituency

Figure: I made this atrocity in Inkscape myself, so now you have to look at it.
Complement-select policy

The paper authors only provided examples where $\log_2(K) = \log_2(N/K)$, but the method works for mismatched lengths of $C$ and $O$ if we treat the comparison appropriately.

- $C = O \rightarrow$ dedicate the set to LRU.
- $C = \overline{O} \rightarrow$ dedicate the set to BIP.
- The remaining sets are follower sets.
Complement-select policy: example 1

\[ N = 2^6, \quad K = 8 \rightarrow \log_2(K) = \log_2(N/K) = 3. \]

<table>
<thead>
<tr>
<th></th>
<th>LRU sets</th>
<th></th>
<th>BIP sets</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C</td>
<td>O</td>
<td>C</td>
</tr>
<tr>
<td>000</td>
<td>000</td>
<td>000</td>
<td>000</td>
</tr>
<tr>
<td>001</td>
<td>001</td>
<td>001</td>
<td>001</td>
</tr>
<tr>
<td>010</td>
<td>010</td>
<td>010</td>
<td>010</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>111</td>
<td>111</td>
<td>111</td>
<td>111</td>
</tr>
</tbody>
</table>
Complement-select policy: example II

\[ N = 2^5, \ K = 4 \rightarrow \log_2(K) = 2, \ \log_2(N/K) = 3. \]

<table>
<thead>
<tr>
<th>LRU sets</th>
<th>BIP sets</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>O</td>
</tr>
<tr>
<td>00</td>
<td>000</td>
</tr>
<tr>
<td>01</td>
<td>001</td>
</tr>
<tr>
<td>10</td>
<td>010</td>
</tr>
<tr>
<td>11</td>
<td>011</td>
</tr>
</tbody>
</table>

Alternatively the MSB in O could be changed in either of those, as long as there is one per constituency.
Complement-select policy: example III

\[ N = 2^5, \ K = 8 \rightarrow \log_2(K) = 3, \ \log_2(N/K) = 2. \]

<table>
<thead>
<tr>
<th>LRU sets</th>
<th>BIP sets</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>O</td>
</tr>
<tr>
<td>000</td>
<td>00</td>
</tr>
<tr>
<td>001</td>
<td>01</td>
</tr>
<tr>
<td>010</td>
<td>10</td>
</tr>
<tr>
<td>011</td>
<td>11</td>
</tr>
<tr>
<td>100</td>
<td>00</td>
</tr>
<tr>
<td>101</td>
<td>01</td>
</tr>
<tr>
<td>110</td>
<td>10</td>
</tr>
<tr>
<td>111</td>
<td>11</td>
</tr>
</tbody>
</table>
We’ll consider two DIP-SD variants for the 1MB L1 cache from earlier.

- $N = 1024$
- $K = 32$
- 10-bit PSEL

- $N = 1024$
- $K = 64$
- 11-bit PSEL

Where not specified, DIP is assumed to mean DIP-SD with $K = 32$. 
Figure: amean: reduction in arithmetic mean of MPKI of all the benchmarks.
n: K from previous slides about SD.
DIP-Global: initial concept with complete ATDs for every set.
Analyzing PSEL changes

For 10-bit PSEL:
- PSEL $\geq 512 \rightarrow$ BIP
- PSEL $< 512 \rightarrow$ LRU

DIP can adapt to changes during a program’s runtime. We can observe this effect by tracking the PSEL value.
Analyzing PSEL changes: mcf

**Figure:** Vertical: PSEL value, horizontal: instructions in millions
Analyzing PSEL changes: health

**Figure**: Vertical: PSEL value, horizontal: instructions in millions
Analyzing PSEL changes: swim

Figure: Vertical: PSEL value, horizontal: instructions in millions
Analyzing PSEL changes: ammp

**Figure:** Vertical: PSEL value, horizontal: instructions in millions
Analyzing the effects of policy change and cache size change

**Figure**: avg: Arithmetic mean MPKI for all the benchmarks, avgNomcf: Same as avg, but without mcf
Additional consideration: bypassing instead of LIP

In BIP as proposed so far, lines were inserted in either the MRU or LRU position. What if in the latter case we skipped inserting the line at all?
Additional consideration: bypassing instead of LIP

Figure: (n) means n% bypassed misses in DIP-Bypass.
### Simulated system configuration

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Machine width</td>
<td>4 instructions/cycle, 4 functional units</td>
</tr>
<tr>
<td>Inst. window size</td>
<td>32 instructions</td>
</tr>
<tr>
<td>Branch predictor</td>
<td>Hybrid 64k-entry gshare, 64k-entry PAs misprediction penalty is 10 cycles min.</td>
</tr>
<tr>
<td>L1-I cache</td>
<td>16kB, 64B block, 2-way with LRU repl.</td>
</tr>
<tr>
<td>L1-D cache</td>
<td>16kB, 64B block, 2-way, 2 cycle hit</td>
</tr>
<tr>
<td>L2 unified cache</td>
<td>1MB, 64B block, 16-way, 6 cycle hit</td>
</tr>
<tr>
<td>Main memory</td>
<td>32 banks, 270 cycle bank access</td>
</tr>
<tr>
<td>Off-chip bus</td>
<td>Proc. to bus speed ratio 4:1, 8B/bus-cycle</td>
</tr>
</tbody>
</table>
Figure: IPC improvement with DIP over LRU. gmean: geometric mean.
Hardware considerations

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Hardware considerations

SetIndex[9:0] Tag DataBus

~PSEL[MSB]

BIPCTR == 0

1

N/A

00

01

10

11

EXISTING CACHE MODULE

Update recency at insert

dedicated_LRU_set
(SetIndex[9:5] == SetIndex[4:0])

dedicated_BIP_set
(SetIndex[9:5] == ~SetIndex[4:0])
Conclusions

- The commonly used (Pseudo-)LRU cache policy performs well for working sets that are no larger than the cache, but suffers from thrashing otherwise.

- BIP solves the thrashing cases, but at the cost of severe performance loss with workloads that benefit from traditional LRU.

- DIP, a hybrid policy which adapts to the workload, performs better than either of the two policies it’s made up of with minimal hardware changes.
